ABSTRACT OF THE DISCLOSURE

The present invention provides a data processor operating in a card host in such a manner as to easily eliminate access errors attributable to propagation delays of a clock signal and data. A memory card interface controller transmits a clock signal to a memory card to acquire read data therefrom in synchronism with the clock signal, the memory card interface controller being switchable between a raising edge and a falling edge of the clock signal when acquiring the read data in synchronous relation with the clock signal. It is possible to adjust a timing of read data acquisition by a half cycle of the clock signal. The memory card interface controller may be switched between different frequencies of the clock signal. Additional switching of frequencies provides more flexibility for timing adjustment.